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09/577,012	05/24/2000	Mohan Kalkunte	P108339-9017	5213

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EXAMINER	
MOORE, IAN N	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,012	KALKUNTE ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *16-29* is/are withdrawn from consideration.

5)☒ Claim(s) *13-15* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102(b)

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-3 and 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Onishi et al (US Patent 5,434,863).

With regard to claim 1, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (first data port interface) (column 7, lines 31-33). Onishi et al further discloses a communication port 54 of token ring LAN as LAN of 4-16 Mbps (second data port interface) (column 7, lines 33-34). Onishi et al further discloses a router manager 2 (flow control unit) that distributes a routing table to routing accelerators 3 that perform route selection (distribute a data load) on the basis of the routing table (column 7, line 9-15). Onishi et al further discloses a bus 4 (trunk group) (column 7, lines 17-18). The bus 4 accommodates communication port 53 and communication port 54; therefore, it is inherent that it has a larger capacity than either port individually.

With regard to claim 2, Onishi et al further discloses a router manager 2 that acts as a main processor (CPU) (column 7, line 4-6). The routing manager 2 is connected (CPU interface) to the router bus 1 (communication channel) (column 7, lines 3-4). With regard to claim 3, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (Ethernet data port interface) (column 7, lines 31-33). With regard to claims 8 and 9, Onishi et al further

discloses that the router manager 2 is connected (CPU interface) to the router bus 1 (communication channel) (column 7, lines 3-4). Onishi et al further discloses that the router manager has the function of managing the whole system and the function of producing/distributing a routing table (program the operation) (column 7, lines 4-6).

With regard to claims 10 and 11, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (maximum of 100 Mbps) (column 7, lines 31-33). A rate of 10 Mbps is included in the range 0-100 Mbps.

Claim Rejections - 35 USC § 102 (e)

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 and 6-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Haddock et al (US Patent 6,104,700).

With regard to claim 1, Haddock et al discloses an octal fast Ethernet interface (first data port interface) (column 4, lines 23-25 and Figure 1A). Haddock et al further discloses a gigabit Ethernet interface 105 (second data port interface) (column 4, lines 19-23 and Figure 1A). Haddock et al further discloses a filtering/forwarding engine 115. Haddock et al further discloses that the filtering /forwarding engine includes a switch matrix (trunk group) (column 4, line 27). The switch matrix connects each channel to a central memory, packet RAM 125, and a

buffer manager (flow control unit) that controls and coordinates access (distribute a load) to and from the packet RAM 125 (column 4, lines 30-34). Switch matrix (trunk group) accommodates octal fast Ethernet interface and a gigabit Ethernet interface 105; therefore, it is inherent that it has a larger capacity than either interface individually.

With regard to claim 2, Haddock et al further discloses that a CPU 130 (applicant's CPU) is coupled (applicant's CPU interface) to the forwarding/filtering engine 115 that includes a switch matrix (communication channel) (column 4, lines 1518 and column 4, line 27).

With regard to claim 3, Haddock et al further discloses an octal fast Ethernet interface 110 (Ethernet data port interface) (column 4, lines 23-25 and Figure 1A).

With regard to claim 4, Haddock et al further discloses a gigabit Ethernet interface 105 (gigabit Ethernet data port interface) (column 4, lines 23-25 and Figure 1 A).

With regard to claim 6, Haddock et al further discloses a forwarding database 120 that stores information useful for making layer 2 decisions (layer two switching) (column 4, lines 35-37).

With regard to claim 7, Haddock et al further discloses a forwarding database 120 that stores information useful for making layer 3 decisions (applicant's layer three switching) (column 4, lines 35-37).

With regard to claims 8 and 9, Haddock et al further discloses that a CPU 130 (CPU) is coupled (CPU interface) to the forwarding/filtering engine 115 that includes a switch matrix (communication channel) (column 4, lines 15-18 and column 4, line 27). Haddock et al further discloses a packet RAM 125 for adapting (program the operation) between incoming and outgoing bandwidth differences (column 4, lines 48-50).

With regard to claims 10 and 11, Haddock et al further discloses an octal fast Ethernet interface 110 (column 4, lines 19-23 and Figure 1A). Data rates of 10/100 Mbps are supported.

With regard to claim 12, Haddock et al further discloses a gigabit Ethernet interface 105 (column 4, lines 19-23 and Figure 1A). A gigabit Ethernet interface supports a data rate of 1000 Mbps.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi et al (US Patent 5,434,863).

With respect to claim 5, Onishi et al does not teach the placement of the first data port interface, second data port interface, CPU interface and communication channel on a single integrated chip. A person of ordinary skill in the art would have been motivated to integrate these components onto a single chip by the constant desire for smaller integrated electronic devices. At the time the invention was made, therefore, have been obvious to one of ordinary skill in the art to integrate these components onto a single chip as specified in claim 5.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock et al (US Patent 6,104,700).

With respect to claim 5, Haddock et al does not explicitly teach the placement of the first data port interface, second data port interface, CPU interface and communication channel on a single integrated chip. A person of ordinary skill in the art would have been motivated to integrate these components onto a single chip by the constant desire for smaller integrated electronic devices. At the time the invention was made, therefore, have been obvious to one of ordinary skill in the art to integrate these components onto a single chip as specified in claim 5.

Allowable Subject Matter

8. Claims 13-15 are allowed.

Response to Arguments

9. Applicant's arguments filed 4/22/05 have been fully considered but they are not persuasive.

Response to First Set of argument

Regarding claims 1-12, the applicant argued that, "...Onishi fails to disclose or suggest that "at least one of said first data ports and at least one of said second data ports are linked together with a plurality of ports on a second network switch forming a trunk group with a larger load capacity than either of said at least one of said first data ports and said at least one of said second data ports, said trunk group being configured by the flow control unit to statistically distribute a data load transmitted across said trunk group"...as presented in claim 1.." in page 3, last paragraph; page 4, first paragraph and last paragraph; page 8, paragraph 4.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Onishi discloses at least one of said first data ports (see FIG. 1, Ethernet port 53; see col. 7, line 31-33) and at least one of said second data ports (see FIG. 1, Token ring LAN port 54; see col. 7, line 33-34) are linked together with a plurality of ports (see FIG. 1-2; each router has pluralities of ports) on a second network switch (see FIG. 2, Router A, C, D, or E; linking to ports of remote routers; see col. 2, line 7-32) forming a trunk group (see FIG. 1, bus 4) with a larger load capacity than either of said at least one of said first data ports and said at least one of said second data ports (see col. 7, line 17-18; bus 4 commodes communication port 53 and 54; therefore, it has a larger capacity than either port individually), said trunk group being configured by the flow control unit (see FIG. 1, Router Manager 2) to statistically distribute a data load transmitted across said trunk group (see col. see col. 7, line 9-15; Manager 2 distributes a routing table to routing accelerators 3 that performs route selection (statically distribution a data load) on the basis of routing table).

The applicant argued that, "...A trunk group according to the claimed invention, is where multiple ports are combined to form a signal **logical** port..." in page 4, paragraph 1.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **logical**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant argued that, "...applicant asserts...that a bus does not correspond to a trunk group..." in page 4, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. In particular, the functionality of a "a trunk group" is to group/combine/multiplex the ports; identically, the functionality of a "bus 4" is to group/combine/multiplex the ports. Thus, it is clear that a bus corresponds to a trunk group.

The applicant argued that, "...Onishi cannot disclose forming a trunk group with a larger load capacity..." in page 5, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in above response, a trunk group corresponds to a bus. Since a bus 4 groups/combines/multiplexes 100 Mbps and 4-16 Mbps ports, it is clear that it has a larger capacity than either 100 Mbps port or 4-16 Mbps ports.

Moreover, the teaching of "high speed bus" with a larger capacity than either first port or second port, is well established in the art as recited in prior art. In particular, Wilson (US005499341A) teaches a high speed bus 13 (see FIG. 1) which groups/combines/multiplexes I/O cards 16, and the high speed bus having a "high" or "large" speed/capacity (see Abstract and col. 5, line 36-59).

The applicant argued that, "...Onishi does not disclose or suggest the use of trunks and thus one of skill in the art **would not have been motivated to modify** Onishi to yield the claim invention..." in page 5, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in previous office action, the rejection of claim 1 is based upon

U.S.C. 102(b) and clearly examiner is not modifying or changing Onishi's system, thus the examiner is not require to disclose any motivation.

Regarding claim 5, the applicant argued that, "...it would not have been obvious to one of skill in the art to integrate the components onto a single chip that included the **trunk group element**..." in page 8, paragraph 3.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **trunk group element**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim 5, line 1 recites, "**a network switch**" is further defined by having components integrated on a single chip, **rather than** "**the trunk group element**" is further defined to have components integrated on a single chip. Thus, it would have been obvious to one of skill in the art to integrate the components onto a single chip that included the network switch.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that Onishi reference as set forth in the rejections are proper.

Response to Second Set of argument

Regarding claims 1-12, the applicant argued that, "...Haddock fails to disclose or suggest that "at least one of said first data ports and at least one of said second data ports are linked together with a plurality of ports on a second network switch forming a trunk group with a larger load capacity than either of said at least one of said first data ports and said at

least one of said second data ports, said trunk group being configured by the flow control unit to statistically distribute a data load transmitted across said trunk group"...as presented in claim 1.." in page 6, paragraph 2-3; page 8, paragraph 4.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Haddock discloses at least one of said first data ports (see FIG. 1A, Octal Fast Ethernet Interface 110; see col. 4, line 23-25) and at least one of said second data ports (see FIG. 1A, Gigabit Ethernet 105; see col. 4, line 19-23) are linked together with a plurality of ports (see FIG. 1A, plurality of ports on switch 100 on LAN) on a second network switch (see col. 1, line 65 to col. 2, line 5; see col. 3, line 45-50; see col. 4, line 31; linking to ports of remote switch in the LAN) forming a trunk group (see FIG. 1A, Switch Matrix) with a larger load capacity than either of said at least one of said first data ports and said at least one of said second data ports (switch matrix accommodates octal fast Ethernet interface and a gigabit Ethernet interface 105; therefore, it has a larger capacity than either interface individually), said trunk group being configured by the flow control unit (see FIG. 1A, Central memory, packet RAM 125 and a buffer manager) to statistically distribute a data load transmitted across said trunk group (see col. 4, line 30-34; controls and coordinates access (statically distribute a load) to and from the packet RAM 125).

The applicant argued that, "...A trunk group according to the claimed invention, is where multiple ports are combined to form a signal **logical** port..." in page 6, paragraph 3 and "...Haddock makes no mention of combining the **channels** to from a trunk group..." in page 7, paragraph 2.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **logical** or channels) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant argued that, "...it would appear that Haddock does not disclose supporting both an octal fast Ethernet interface and a gigabit Ethernet interface at the same time..." in page 7, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Applicant is arguing the uses of channels in the switch, and the uses of channels are not disclosed in the claim. As examiner asserts in the previous office action, "a trunk group" has the same functionally as "switching matrix". Clearly, from viewing FIG. 1A of Haddock, one can easily see that switch matrix combines/groups input and outputs of each ports (Fast and Gigabit rates), thus it is clear that the switch matrix has a larger capacity than either Fast or Gigabit Ethernet speed/rates.

Moreover, the teaching of "switching matrix" with a larger capacity than either first port or second port, is well established in the art as recited in prior arts as follows:

- Jeong (US005774665A) teaches a switching matrix module 2 (see FIG. 1) which groups/combines/multiplexes interface modules 1,3,4-7, and the switch matrix having a capacity large enough to switch different types of data (see Abstract, see FIG. 4, and col. 2, line 55 to col. 3, line 7; 57-67).

- Dahod (US5682383) teaches a switch matrix 200 (see FIG. 3) which groups/combines/multiplexes interfaces 126-1 to 126-8 and 150-1 to 150-3, and the switch matrix having a capacity large enough to switch different types of data (see Abstract, see FIG. 4, and col. 4, line 19-46).
- Szczepanek (US006690668B1) teaches a crossbar-switch matrix 100 (see FIG. 12) which groups/combines/multiplexes interfaces 20-1 to 20-16, and the switch matrix having a capacity large enough to switch different types of data (see Abstract, and col. 23, line 10-64).

The applicant argued that, "...Haddock does not disclose or suggest the use of trunks and thus one of skill in the art **would not have been motivated to modify** Onishi to yield the claim invention..." in page 7, paragraph 3.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in previous office action, the rejection of claim 1 is based upon U.S.C. 102(b) and clearly examiner is not modifying or changing Haddock's system, thus the examiner is not require to disclose any motivation.

Regarding claim 5, the applicant argued that, "...it would not have been obvious to one of skill in the art to integrate the components onto a single chip that included the **trunk group element**..." in page 9, paragraph 1.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **trunk group element**) are not recited in the rejected claim(s). Although the claims are interpreted

in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim 5, line 1 recites, "**a network switch**" is further defined by having components integrated on a single chip, **rather than** "**the trunk group element**" is further defined to have components integrated on a single chip. Thus, it would have been obvious to one of skill in the art to integrate the components onto a single chip that included the network switch.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that Haddock reference as set forth in the rejections are proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
9/1/05

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